Detector Support Group
Weekly Report, 2019-11-20

Summary

Hall A – SoLID Solenoid Controls

- Designing of *Constant Current Source* (CCS) board to provide fixed current for temperature sensors in the solenoid
  - ✶ Updated original parts list for the 100uA version of the CCS pcb
  - ✶ Ensured all parts list's components were available for purchase
  - ✶ Completed parts generation and preliminary schematic layout in Altium
- Developing FactoryTalk View data logger
- Completed project schedule spreadsheet

Hall B – RICH

- Performed maintenance of compressor # 2 used for the electronic panel's cooling system
  - ✶ Inspected air filters – clean and not damaged
  - ✶ Verified correct tension for the belt set, ensured deflection was 5 mm—7 mm when exerting a force of 25 N
  - ✶ Noted compressor run time local display 580 hours
  - ✶ Next scheduled maintenance must take place at 1000 compressor running hours
  - ✶ Turned compressor on and confirmed that pressure settings and flow rates were correct

Hall B – HDice

- Conducted meeting to review operation of Lock-in Amplifier for NMR signal measurement
  - ✶ Agreed that HDice will demonstrate to DSG the operation, features used, and needed functionality of the new lock-in amplifier when the test setup is ready

Hall B – BoNuS Target Gas Controls

- Started testing control software on spare cRIO
  - ✶ Found that shared variables don't update at the rate expected on some VIs

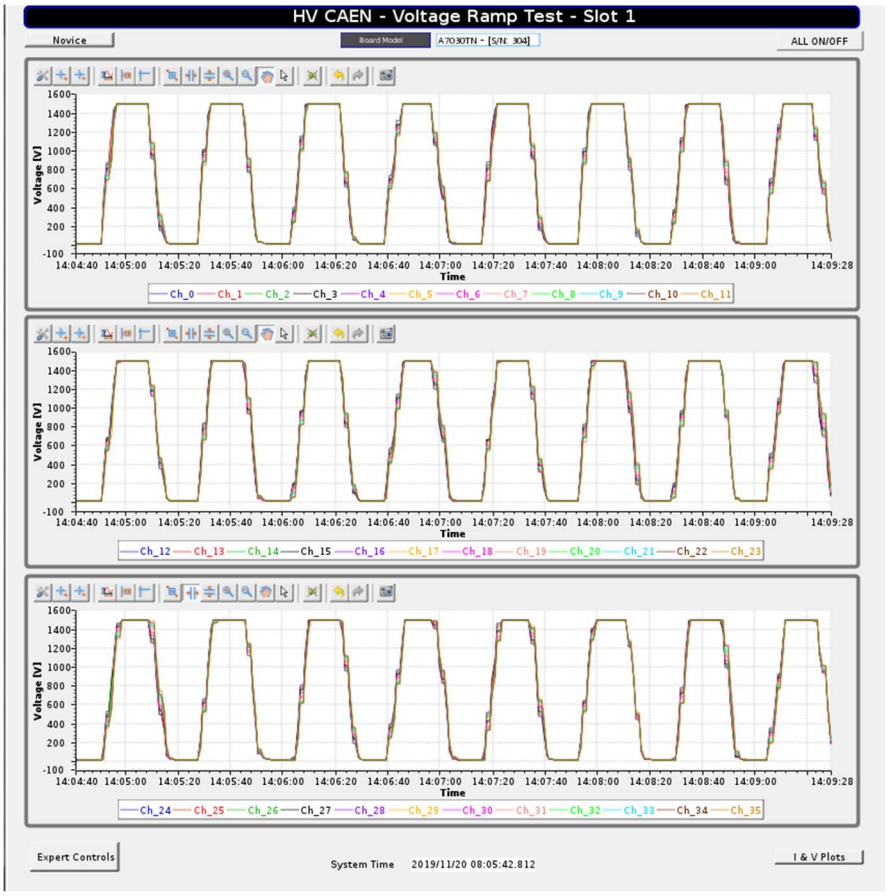
Hall B – RTPC

- Debugged MPOD crate network communication issues
  - ✶ MPOD's MAC address was reset when firmware was changed
- Added 75' extension cable for one of the RTDs glued into the detector

Hall C – CAEN EPICS Test Station

- Testing A7030TN board with updated firmware (rev. 1.06)
  - ✶ Upgraded A7030TN board (Ser. #: 304)
  - ✶ Repeated automated test by using GECO 2020
    - ▪ Used GECO 2020 script to ramp up/down 36 channels, simultaneously for 300 times
    - ▪ Used GECO 2020 data logger advanced feature to record 10 parameters
  - ✶ Enabled CAEN EPICS server to allow only monitoring of the test via *Voltage Ramp Test- Slot 1* CSS-BOY screen

- Results of the test showed no latency to ramp for all 36 channels



Zoom-in view of *Voltage Ramp Test CSS-BOY* screen shows no latency issues

Hall C – CAEN HV Test Station

- Testing CAEN-A7030TN boards
  - Tested all 36 channels on boards (Ser. # 0304 and 0326)
  - Test conducted with just a single board in slot 0, data analysis in progress

Engineering Division

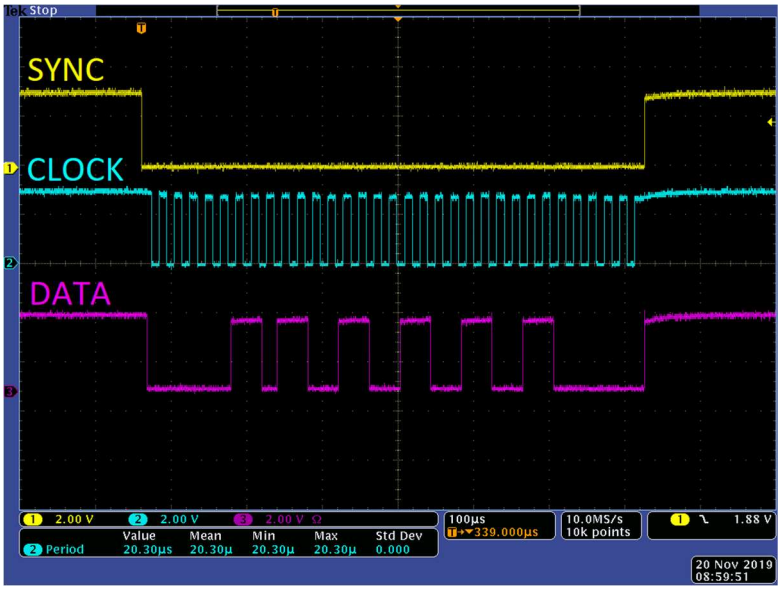
- Soldered LEDs, headers (three types), varistors, LEMO connectors, fuse holders, and OPTP receivers for the Beam Position Monitor boards

DSG R&D – RICH

- Prototyping Sensirion SHT85 integrated temperature/humidity sensor power supply distribution scheme, interconnections, and signal distribution for the sbRIO
  - Fabricating RJ45 power and sensor signal distribution panel prototype
  - Received and tested production cable assemblies for SHT85 sensors
  - Tested data signal termination assembly for NI 9694 sbRIO FPGA interface
  - Integrated sensor and termination DC (24V) - DC (3.3V) power supply and tested sensors and sbRIO
- Added subVI to SHT85 user interface to count number of out-of-limit reading

DSG R&D – LV Chassis FPGA

- Investigated timing requirements for DAC communication
- Used schematic for LV chassis DE0 breakout board and sensor readback board to wire sbRIO output to LV Chassis DAC
- Developed subVI to generate clock, sync, and data signals for DACs on sbRIO FPGA
    - ✶ SubVI successfully tested by setting DAC in LV chassis.



Oscilloscope screenshot of clock, sync, and data signals generated by FPGA. Data signal is command to set DAC output of channel 7 to 2 V

DSG R&D – PLC Test Station

- Developing test for analog input and output modules